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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/359,056	07/21/1999	BARMAK MANSOORIAN	08305/038001	2286

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Thomas J D'Amico
Dickstein Shapiro Morin & Oshinsky LLP
2101 L Streew NW
Washington, DC 20037-1526

EXAMINER	
TRAN, NHAN T	
ART UNIT	PAPER NUMBER
2615	

DATE MAILED: 07/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/359,056	MANSOORIAN, BARMAK	
	Examiner	Art Unit	
	Nhan T. Tran	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *5/4/2005 & 4/4/2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,4,6 and 8-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *14 and 17* is/are allowed.

6)☒ Claim(s) *1,3,4,6,8-13,15 and 16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *1/7/2004 & 7/21/1999* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 5/4/2005 & 4/4/2005 has been entered.

Response to Arguments

2. Applicant's arguments with respect to claims 1, 3, 4, 6, 8-13, 15 & 16 have been considered but are moot in view of the new ground(s) of rejection.

Drawings

3. New corrected drawings in compliance with 37 CFR 1.121(d) are required in this application because the drawings filed 1/7/2004 & 7/21/1999 are informal. Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 3, 4, 6, 8-13, 15 & 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pain et al (US 5,886,659) in view of Long et al (US 5,811,984) and in further view of Pickering et al (US 5,050,194).

Regarding claim 1, Pain discloses an image sensor comprising:

an image acquisition portion (100, 112) as shown in Figs. 1A-1C, col. 3, lines 52-63;

an image processing portion (ADC array 118), receiving image information from said image acquisition portion, said image processing portion including a CMOS circuitry with CMOS outputs having an output impedance; said image processing portion producing a current mode output (see Fig. 1C; col. 1, line 55 – col. 2, line 7; col. 5, line 65 – col. 6, line 5 & col. 7, lines 10-16). It is noted that the output impedance is inherent at the ADC array output. Since the ADC array is configured with CMOS current driving mode, the impedance must exist at the ADC array output and throughout transmission line(s).

Pain also implicitly discloses (Figs. 1A-1C) another separate portion (i.e., another chip) to be connected to an output of ADC array for receiving digital image data output from the ADC array. The implied separate portion represents "an image receiving portion, having an input impedance, receiving said image information from said CMOS outputs, and said image receiving

portion receiving current mode output" in order to form a complete imaging system of CMOS compatible applications (see col. 2, lines 5-7 for a consistent CMOS compatible imaging system).

Therefore, it would have been obvious to one of ordinary skill in the art to recognize another chip connected to the digital output from the image processing portion (ADC array 118) as an image receiving portion which would be also configured in CMOS having input characteristics being compatible with the digital output of the image processing portion in a complete imaging system.

Pain does not explicitly disclose the CMOS outputs being differential outputs and that an image receiving portion has at least a pair of transistors and an active impedance matching device having a current source being adapted to match said output impedance of said image processing portion to said input impedance of said image receiving portion by adjusting, with said current source, a bias current through said at least a pair of transistors.

Long teaches an active impedance matching device (Figs. 3 & 4) having a current source (70). See col. 2, line 50 – col. 3, line 47. Long teaches that the active impedance matching device is implemented in CMOS and being adapted to match an output impedance of transmitter of a chip (40) to an input impedance of receiver of another chip (42) by adjusting, with the current source, a bias current through at least a pair of transistors (see col. 4, lines 10-63, wherein at least a pair of transistors is shown in a detailed circuit of receiving chip 42 in Fig. 4). Such an implementation of CMOS current mode driver and an active impedance matching device reduces power dissipation in digital circuits by transmitting current mode signal with relatively small current swings (see col. 2, lines 38-40 and col. 4, lines 10-15).

Therefore, it would have been obvious to one of ordinary skill in the art to combine the teachings of Pain and Long to construct an image sensor having an image receiving portion having at least a pair of transistors and an active impedance matching device having a current source for actively matching an output impedance of an image processing portion to an input impedance of an image receiving portion operated with relatively small current swings by adjusting with a current source a bias current through at least a pair of transistors so that power dissipation would be reduced.

Pain and Long are silent about CMOS differential outputs of the image processing portion. Pickering teaches a CMOS differential output implemented as a CMOS differential output driver (see Pickering, Fig. 1) for driving current mode signals over a transmission line (5) between chips (see col. 2, lines 45-50). The CMOS differential output provides advantage of minimizing the effects of common-mode noise beside the advantage of matching impedance (see Pickering, col. 2, lines 16-20).

Therefore, it would have been obvious to one of ordinary skill in the art to further modify the combination of Pain and Long with the teaching of Pickering to incorporate a differential output/input driver using CMOS technology for transmitting and receiving off-chip image data with reduction in common-mode noise.

Regarding claims 3 & 6, the combination of Pain, Long and Pickering shows that the impedance matching device comprises a circuit (circuit 46, Fig. 3 in Long or circuit 3, Fig. 1 in Pickering) on the image processing portion (transmitter) and also comprises a circuit (circuit 52, Fig. 3 in Long or circuit 8, Fig. 1 in Pickering) on the image receiving portion (receiver).

Regarding claim 4, it is also clear in the combination of Pain, Long and Pickering that an output circuit of an image processing (transmitter) includes a transistor adapted to receive a current bias, wherein the magnitude of the current bias sets the output impedance of the image processing portion (see Long, Fig.3 and col. 4, lines 31-40 or Pickering in Fig. 1 at block 3).

Regarding claim 8, see the analysis of claim 1. Furthermore, both Long and Pickering discloses that a current mode driver having an output voltage swing of less than 0.5 volts. See Long, col. 4, lines 31-40, col. 3, lines 40-43 and Table II in col. 7, wherein current swings of 1mA must generates a relatively low voltage swings of less than 0.5 volts at the output of transmitter 40 over transmission line 44 since it is required a current swings between 10 mA to 40 mA to generate a voltage swings of at least 0.5 volts (see col. 1, lines 25-55). Also see Pickering in col. 2, lines 55-58 for a 250 mV (.25 volts) differential voltage swing on 50 Ohm transmission line.

Regarding claim 9, see the analyses of claims 3 & 6.

Regarding claim 10, see the analysis of claim 4 and Long, col. 4, lines 54-63.

Regarding claim 11, see the analyses of claims 1 & 8, wherein image acquisition portion is considered as portion 112 in Fig. 1C in Pain and image processing portion is considered as an implied "another portion" at output 110. Also, the active impedance matching device taught in

Long renders input impedance relatively independent of an input current by adjusting bias current through at least one biased device (Long, col. 2, lines 60-63).

Regarding claim 12, the combination of Pain, Long and Pickering teaches the image receiving portion including a current source for biasing transistors as analyzed in claim 4. Pain, Long and Pickering do not specifically disclose that the current source is a current mirror part. However, an Official Notice is taken that a current source can be configured by a current mirror in CMOS application. Therefore, it would have been obvious to one of ordinary skill in the art to configure a current source using a well-known current mirror to generate current for the circuit.

Regarding claim 13, Pain discloses the image acquisition circuit being an active pixel sensor (APS 300) with a photosensor (photogate 310), an in-pixel buffer (floating diffusion 330, transistor 360), and in-pixel select transistor (vertical select 370) (see Fig. 3A; col. 6, lines 25-49).

Regarding claim 15, see the analyses of claims 1 & 11.

Regarding claim 16, see the analyses of claims 1 & 11.

Allowable Subject Matter

5. Claims 14 & 17 are allowed.

The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record fails to teach or fairly suggest the **combination of all limitations** required in each of claims 14 and 17 that includes the limitation of *the image acquisition portion and the image processing portion operate at substantially zero voltage*.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nhan T. Tran whose telephone number is (571) 272-7371. The examiner can normally be reached on Monday - Thursday, 8:00am - 6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Ometz can be reached on (571) 272-7593. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NT.

DAVID L. OMETZ
PRIMARY EXAMINER